IN THE CLAIMS:

Please amend claim 25 as follows:

LISTING OF CURRENT CLAIMS

Claims 1-24. (Canceled)

Claim 25. (Currently Amended) A flip-chip package comprising:

a) a substrate having:
   i) a top substrate surface;
   ii) a bottom substrate surface; and
   iii) a substrate opening extending through the top surface and the bottom surface;

b) a dummy die being a silicon substrate having no electrically calculating function, connected to the bottom substrate surface and aligned with the substrate opening, and having a redistribution layer, the redistribution layer having a plurality of flip-chip pads and a plurality of connecting pads connected by an integrated circuit trace, the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening, the plurality of connecting pads of the redistribution layer are electrically connected to the substrate, wherein the dummy die has an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die; and

c) a chip located in the opening and having a plurality of bumps electrically connected to the plurality of flip-chip pads of the redistribution layer.

Claim 26. (Previously Presented) The flip-chip package according to claim 25, further comprising a package body located in the substrate opening and encasing the chip.

Claim 27. (Previously Presented) The flip-chip package according to claim 25, wherein the substrate is a printed circuit board.

Claim 28. (Previously Presented) The flip-chip package according to claim 25, wherein the dummy die has a size larger than a size of the chip.

Claim 29. (Previously Presented) The flip-chip package according to claim 25, wherein each of the plurality of flip-chip pads have a pitch smaller that a pitch of each of the plurality of connecting pads.

Claim 30. (Previously Presented) The flip-chip package according to claim 25, wherein each of the plurality of flip-chip pads have a pitch less than 150 m.

Claim 31. (Previously Presented) The flip-chip package according to claim 25, further comprising a plurality of bonding wires electrically connecting the plurality of connecting pads to the substrate.

Claim 32. (Previously Presented) The flip-chip package according to claim 25, further comprising a plurality of bumps electrically connecting the plurality of connecting pads to the substrate.

Claim 33. (Previously Presented) The flip-chip package according to claim 25, further comprising a plurality of top connection pads located on the top substrate surface.

Claim 34. (Previously Presented) The flip-chip package according to claim 25, further comprising a plurality of solder balls connected to the bottom substrate surface.

Claim 35. (Previously Presented) The flip-chip package according to claim 33, wherein the plurality of top connection pads of a top flip-chip package are connected to the plurality of bottom solder balls of a bottom top flip-chip package.

Claim 36. (Previously Presented) The flip-chip package according to claim 25, further comprising an adhesive tape connecting the dummy die to the bottom substrate surface.

Claim 37. (Canceled)

Claim 38. (Previously Presented) The flip-chip package according to claim 25, wherein the substrate opening includes a stair located on an interior circumference thereof.

Claim 39. (Previously Presented) The flip-chip package according to claim 25, wherein the metal thermal-conducting layer is a sputtered metal layer.